Notice of References Cited

Application/Control No.

09/975,257

Applicant(s)/Patent Under Reexamination NARAYANAN ET AL.

Examiner

David L. Hogans

Applicant(s)/Patent Under Reexamination NARAYANAN ET AL.

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-6,528,433	03-2003	Gartner et al.	438/786
	В	US-5,904,523	05-1999	Feldman et al.	438/263
	С	US-6,060,374	05-2000	Lin et al.	438/514
	D	US-			
	Ε	US-			
	F	US-			
	G	US-			
	Н	US-			
	1	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	Q					
	R					
	S					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	٦	Quirk et al., Semiconductor Manufacturing Technology (2001), Prentice Hall, page 477.
	V	Wolf et al., Silicon Processing for the VLSI Era (2000), Lattice Press, Second Edition/Volume 1, pages 299, 300 and 310.
	w	Wolf et al., Silicon Processing for the VLSI Era (1995), Lattice Press, Volume 3, pages 311-313 and 649-654.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.